REMARKS

With this amendment, Claims 1-32 are pending in the present application. Claims 1 has been amended. In view of the foregoing amendment and the following remarks, Applicant respectfully requests reconsideration and allowance of this application.

Objections to the drawings

The Examiner disapproved the proposed drawing corrections filed on October 11, 2002 because the Examiner believes that the proposed drawing introduces new matter into the drawing. Applicant respectfully disagrees with the Examiner and would like to direct the Examiner's attention to Claim 17 of the original disclosure in which it is clearly recited that the multichip cube structure has a first integrated circuit chip comprising a lower surface wherein a fourth insulating layer is formed on the lower surface of the first chip. Thus, no new matter is added by the substituted sheet of drawing.

Furthermore, Applicant has also amended the specification to incorporate the features covered by the originally filed Claim 17 into the specification. Applicant is also submitting herewith a SUBMISSION OF PROPOSED DRAWING AMENDMENT FOR APPROVAL BY EXAMINER to add reference numerals to the fourth insulating layer, which do not constitute new matter as the fourth insulating layer is disclosed in Claim 17 of the original disclosure.

Claim Rejections -- 35 U.S.C. § 103

The Examiner maintained his rejection of Claims 1-26 under 35 U.S.C. § 103(a) as being unpatentable over Asada in view of Morinaga. However, Applicant notes that neither reference teaches or suggests forming voids *within* the insulating material positioned between individual chips. One of the novel features of Applicant's invention is the use of a foamed insulating material having enclosed voids formed within the layer as an insulating layer. Applicant's insulating layer not only reduces capacitive coupling between adjacent circuits but also can structurally support individual chips mounted in a stack of a multichip module. Hence, Applicant's insulating layer is particularly suited for use in a multichip module.

Morinaga discloses a method of forming strings or branches on an upper surface of an insulating film positioned between wiring layers of a single chip. The strings or branches are based on growth nuclei formed in the insulating film. Another insulating film is formed on the upper ends of the insulating branches as a layer and supports the upper wiring layer. The strings

and branches support the weight of the wiring layers above, which is significantly lighter than a semiconductor chip. Since these insulating branches have a diameter of less than 1 micron, (*See, e.g.*, Column 2, Lines 35-44), they are unlikely to be able to structurally support the weight of one or more chips without becoming compressed. Thus, Applicant submits that there is not teaching or suggestion in either Morinaga with Asada directed toward a multichip structure having enclosed voids in the insulating layers between chips. In fact, the strings and branches taught in Morinaga are likely to be crushed in a multichip stack disclosed in Applicant's invention.

Moreover, Applicant notes that even Morinaga acknowledges that it is difficult to form holes *within* the interlayer insulating film. (*See, e.g.,* Column 1, Lines 43-52) Morinaga discloses growing strings of insulating material between two insulating films as an alternative to forming holes *within* a film. Applicant's invention, on the other hand, is directed toward the formation of enclosed voids within the insulating material itself. This advantage allows the insulation material to be used in a multichip module because the material would provide adequate structure support between individual chips. Thus, Applicant submits that the pending claims are patentably distinct from the cited references.

CONCLUSION

Hence Applicant respectfully submits that the pending claims are allowable over the cited references and the application is now in condition for immediate allowance and requests the prompt allowance of the same. Should there be any impediment to the prompt allowance of this application that could be resolved by a telephone conference, the Examiner is respectfully requested to call the undersigned at the number shown below.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 3/13/2003

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